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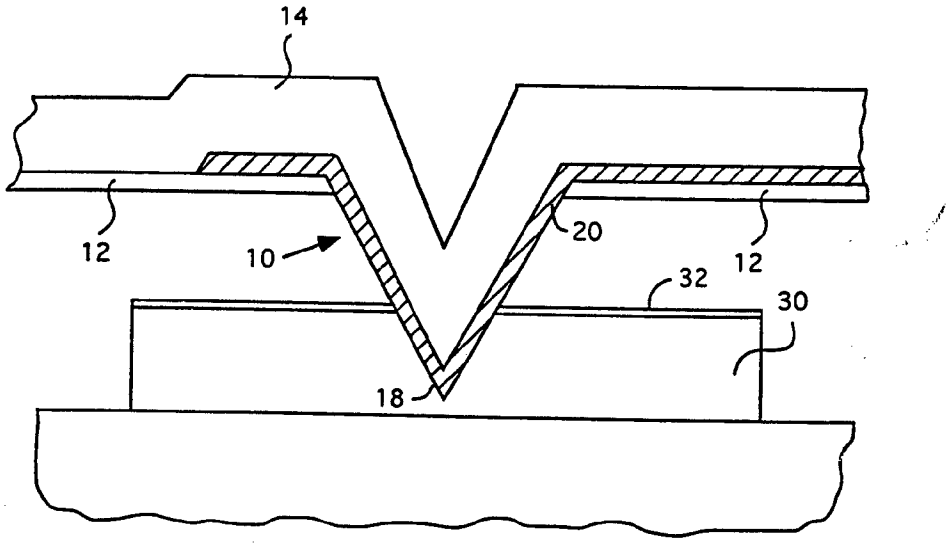

(57) Abstract

A device for making temporary or permanent electrical connections to circuit pads of an integrated circuit is made with conventional semiconductor fabrication processes. The device has a supporting substrate from which project a plurality of insertion structures (10) that are in mating alignment with corresponding circuit pads (30) of the integrated circuit. Each insertion structure is metallized to make electrical contact with the corresponding circuit pad. The electrical contacts may be temporary or permanent depending upon the choice of metallization and the pressure applied to the contacting surfaces. The insertion structure devices have particular application for functional testing, electrical burn-in and packaging of an integrated circuit either as a full wafer or as an individuel die.

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INTERCONNECTION STRUCTURE FOR INTEGRATED CIRCUITS AND METHOD FOR MAKING SAME

SUMMARY OF THE INVENTION

Functional testing, electrical burn-in and packaging of integrated circuits (ICs) have become ever increasingly important aspects of the IC manufacturing process since each of these imposes limitations on the practical complexity of ICs and significantly impacts the cost of electronic goods made with ICs. The present invention reduces the costs associated with present methods of functional testing, burn-in and packaging of ICs by integrating into the highly cost efficient IC fabrication process a novel interconnection device that reduces the complexity and increases the capability of IC functional testing, burn-in and packaging.

The present invention provides a low cost means for making precision placement of electrical interconnections to metal signal, power and ground contacts of arbitrary size on the surface of an IC die through no more than the two steps of physical alignment and the application of a mechanical loading force. Rigid or flexible substrates fabricated with a plurality of insertion structures can be used to make temporary and reliable electrical interconnection to the signal, power and ground contacts of an IC for the purpose of functional testing of all or a portion of an IC, or for the purpose of extended testing often referred to as burn-in. Permanent interconnect IC bonds can be formed with the insertion structure for the purpose of IC packaging.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1a is a cross-sectional view of an insertion structure fabricated in accordance with the present invention.

Figure 1b is a cross-sectional view of the insertion structure of Figure 1a in temporary electrical contact with an integrated circuit pad.

Figure 1c is a cross-sectional view of an insertion structure according to the present invention in permanent electrical contact with an integrated circuit pad.

Figure 2 is a cross-sectional view of a contact device with plural insertion structures.

Figure 3 is a cross-sectional view of an integrated circuit device with an integral insertion structure.

Figure 4a illustrates a circuit probe according to the present invention for use in functional testing or electrical burn-in of an integrated circuit.

Figure 4b is a cross-sectional view of a circuit probe for use in functional testing or electrical burn-in of a full wafer IC.

Figure 5a is a cross-sectional view of an alternative circuit probe fixture.

Figure 5b is a cross-sectional view of an integrated circuit with integral insertion structures in combination with a mating test fixture.

Figure 6 is a cross-section view of a device for mounting and packaging an integrated circuit according to the present invention.

Figure 7 illustrates the fabrication of a three-dimensional integrated circuit structure according to the present invention.

Figure 8 is a cross-sectional view of an insertion structure with an elongated blade tip.

Figure 9 is a cross-sectional view of an insertion structure with a concave tip.

DETAILED DESCRIPTION OF THE INVENTION

In the following description, for purposes of explanation and not limitation, specific details are set forth in order to provide a thorough understanding of the present invention. However, it will be apparent to one skilled in the art that the present invention may be practiced in other embodiments that depart from these specific details. In other instances, detailed descriptions of well-known methods, devices and circuits are omitted so as to not obscure the description of the present invention with unnecessary detail.

Basic Insertion Structure

Referring first to Figure 1a, a basic insertion structure 10 constructed in accordance with the present invention is shown in cross section. Insertion structure 10 has a generally pyramidal shape with opposite sidewalls inclined at an included angle α. A conductive layer 20 is deposited or otherwise formed on the surface of insertion structure 10. As more fully described below, established semiconductor and micro-machining processing techniques and methods are used to form the insertion structure 10 and conductive layer 20.

Using conventional semiconductor processes, insertion structure 10 can be made with geometries from greater than 100μm in extended length *l* and 250μm in maximum diameter feature size to less than 1μm in extended length and 0.5 μm in maximum diameter feature size. The

geometry of the insertion structure is limited only by the capability of available semiconductor processing equipment. The continuing enhancement of semiconductor processing equipment can be expected to permit the fabrication of insertion structures with minimum feature sizes of less than 100nm.

Referring now to Figure 1b, insertion structure 10 is shown in contact with a metal pad 30 such as a bonding pad of an IC. When pressed into the pad 30 by an applied force, the insertion structure 10 penetrates (indents) the surface of the metal pad, including any native oxide 32 formed on the metal surface, and establishes a low resistance electrical contact. The low resistance of the contact results from the penetration of any native oxide or other surface contamination by the insertion structure, and the deformation of the metal pad, thereby increasing surface contact with the insertion structure.

The pointed tip 18 of insertion structure 10 with its conductive layer 20 penetrates a prescribed distance into the metal pad 30. The depth of penetration is determined primarily by the applied load force and the included angle α of the tip of the insertion structure. In addition, the choice of material for the conductive layer 20 on the insertion structure, the value of the included angle α of the insertion structure and the magnitude of the load force are all factors which determine whether the connection between insertion structure 10 and metal pad 30 is temporary or permanent. As an example, an insertion structure coated with approximately 2,000Å of aluminum, with an included angle of 70° and

load force of approximately 1 gm will penetrate an aluminum contact pad to a depth of approximately 5,000Å and form a permanent bond (metal diffusion bond). In contrast, a copper or iridium coated insertion structure under similar conditions will not form a permanent bond, but will maintain a temporary low resistance electrical contact as long as the load force is applied.

A critical aspect of the present invention is fabrication control of the extended length *l* of the insertion structures. The extended length of the insertion structure is measured from the surface of the original substrate in which it is formed. The points or ends of the insertion structures typically penetrate less than 1μm into the surface of the metallized circuit pad with which the insertion structure is intended to make contact. In the typical case of a substrate having a plurality of insertion structures for contact with a corresponding plurality of IC pads, the variation in the extended length of the insertion structures should be less that 50-75% of the desired penetration depth, although greater variation may be acceptable with the use of a thin flexible (membrane) substrate. Flatness variations of the surface of the original substrate over an area of several square centimeters are estimated to be less than 100Å for prime quality silicon wafers. The variation of controlled etch into the substrate is typically less than 0.5% of the extended length of the insertion structures with aspect ratios of 4:1 or less for insertion structures placed over an area of several square centimeters.

A variety of metal films may be used to form the conductive layer on the insertion structure. Some examples are aluminum, copper, iridium or multiple layer films such as iridium:copper, tin-lead:copper or indium:aluminum. The use of tin-lead, indium, indium alloys or other lower melting point metal solders or metal alloys enable permanent bonds to be subsequently debonded with the application of a temperature above the melting point of the metal alloy. The use of a metal conducting layer on the insertion structure that is the same as that used to form the metal contact pad on the IC will allow a permanent metal diffusion bond to occur under appropriately selected loading force and included angle of the insertion structure. Figure 1c illustrates such a permanent bond where, for example, a tin-lead film 21 is applied over insertion structure 10 as well as IC pad 30. The use of dissimilar metals such as iridium, rhodium or copper metals in forming the insertion structure versus an aluminum contact pad on the IC will generally result in a temporary low resistance contact that may be maintained for as long as the appropriate loading force is applied.

Fabrication Methods

The insertion structures of the present invention are formed by etching the desired pattern of projecting structures into a sacrificial substrate. Single crystal silicon with a <100> crystal orientation is the preferred material for the substrate. However, the present invention is not limited to this particular crystal orientation or to the use of silicon as a substrate. Materials such as gallium arsenide, indium phosphide or diamond can

also be used. The primary requirements that the sacrificial substrate must meet are: (i) it can be etched to form the desired insertion structure shapes; (ii) it can be polished to a sufficient flatness tolerance; (iii) it can withstand subsequent processing steps; and (iv) it can be selectively etch removed uniformly in part or whole.

Referring again to Figures 1a and 1b, a mask layer 12 is first deposited on the substrate (not shown). In preferred embodiments of the present invention, mask layer 12 is a dielectric such as silicon dioxide or silicon nitride deposited with a depth of approximately 1000Å to 2500Å and a tensile stress of approximately $1x10^8$dynes/cm^2. A process for making such a deposition is disclosed in this inventor's co-pending application Serial No. 07/865,412 filed April 8, 1992, the specification of which is incorporated herein by reference. Thicker layers of dielectric in excess of 2500Å are best formed with silicon dioxide alone or in combination of two materials such as, for example, 1000Å of nitride, 4μm of oxide and another 1000Å of nitride.

Since the primary function of this dielectric is to act as a mask for etching the underlying substrate, other appropriate mask materials could also be used in lieu of the preferred dielectric materials. Layer 12 is then etched to the underlying substrate with a pattern of windows defining the locations of the insertion structures. The substrate is then etched to create wells for the insertion structures.

The shape of each window defines the cross-sectional shape of the resulting insertion structure, whereas the etching process used determines the inclination of the side walls. For example, a square window with typical wet etch processing will produce a pyramidal insertion structure with a square cross-section. A rectangular window will produce an elongated prismatic insertion structure with a blade-like edge rather than a pointed tip (see Figure 8). Circular, oval or other shaped windows may likewise be employed to produce insertion structures of nearly any desired shape (see Figure 9).

Etch processing of the insertion structures can be accomplished by wet or dry etching techniques or a combination of both. Wet etch processing of silicon is performed typically with potassium hydroxide (KOH) or tetra methyl ammonia hydroxide (TMAH) to achieve anisotropic etching profiles in a <100> single crystalline silicon substrate. Etching with KOH or TMAH produces an insertion structure with an included angle of approximately 70°. Dry etch processing may be used to produce larger or smaller included angles in forming the desired shape of the insertion structures. Dry etch processing can be used to fabricate insertion structures of widely varying form as discussed below.

After the insertion structure shape has been etched into the substrate, conductive layer 20 is deposited using, for example, aluminum, iridium-copper, or SnPb-Cu. The thickness of the deposited metal is selected by the electrical contact result desired and the structural requirements of the contact to be made; e.g. a thicker deposition of metal is required if a

subsequent layer of dielectric material is not deposited, or the hardness of the initial deposited metal layer may require the deposition of a second metal layer of appropriate hardness and/or a dielectric layer. Deposited metal film thickness will typically vary between 1,000Å and 4μm. The metal deposition is patterned in accordance with the individual insertion structures. Optionally, additional dielectric and metal films can be deposited and patterned to interconnect the insertion structures with one another and/or with other circuit elements. Care is taken to isolate the metal insertion structure from contact with remaining portions of the semiconductor substrate as shown, for example, in Figures 2 and 8.

Following deposition of conductive layer 20 and any additional metal/dielectric circuit layers, a structural layer 14 of dielectric material is preferably deposited to enhance durability of tip 18 and to achieve a desired electric signal impedance characteristic between adjacent insertion structures or circuit elements. The thickness and stress characteristics of structural layer 14 (and all other dielectric layers) are selected as appropriate for subsequent use of the insertion structures on a flexible, membrane or thinned substrate. Such structural inorganic materials as diamond, polysilicon, silicon carbide, silicon nitride, aluminum nitride, or organic polymeric materials such as polyimides or parylene may be deposited. As mentioned previously, the preferred materials are silicon dioxide and silicone nitride deposited with a tensile stress of approximately $1x10^8 dynes/cm^2$.

Flexible, membrane or thinned substrates typically vary in thickness from 1000Å to 10μm or more depending on the desired use. Optionally, the surface of the substrate with the insertion structures may be bonded to a second rigid substrate or backing substrate. This bonding process can be accomplished for example by metal diffusion, or SiO_2 anodic bonding techniques. The original substrate in which the insertion structures were formed is subsequently partially or completely removed (as shown in Figures 2 and 1a, respectively) by a highly uniform and selective process of etching or a combination of grinding and selective etching. This leaves the insertion structures exposed to some portion of their extended length.

The side of the flexible or rigid substrate with the exposed insertion structures may be subjected to additional processing steps. These processing steps may include additional metallization interconnect and dielectric films and a passivation film. This provides the capability for fabrication of additional interconnect metallization structures on the backside of an IC, such as 46 shown in Figure 2.

Exemplary Embodiments

The basic insertion structure described above has numerous variations and applications for testing, burn-in and packaging of ICs, some of which are described below with reference to Figures 2-9.

Figure 2 illustrates a contact composed of two insertion structures 10 so as to maximize the contact surface area with a single metal contact or

bonding pad of an IC. The insertion structures are supported by a rigid backing substrate 40 bonded to dielectric layer 14. Planarizing dielectric 42 is deposited within depressions in layer 14 above the insertion structures to provide a flat bonding surface. One or more additional metallization layers 46 may be deposited to provide circuit connections to the conducting layer 20.

In Figures 2 and 3, a portion of the sacrificial substrate 44 remains below dielectric film 12 which can be utilized for fabrication of an integrated circuit integral with the insertion structures. The remaining portion of the substrate is a circuit device grade epitaxial layer formed over a germanium-boron (GeB) doped epitaxial layer, or other etch stop means such as an implanted layer of silicon dioxide or silicon nitride, which is used as a highly uniform (selective) etch stop in removing the original silicon substrate. GeB doped to a concentration of approximately $2x10^{20}$boron atoms/cm^3 provides a particularly effective etch stop for KOH or TMAH, having a selectivity over silicon in the range of approximately 1000-5000:1 depending on the exact doping concentration. The germanium co-doping of approximately 1-1/2% provides stress relief in the epitaxial film. The GeB epitaxial etch stop layer is typically less than 1.5μm in thickness. The GeB etch stop layer is (optionally) subsequently removed to expose the circuit device grade epitaxial layer for additional IC fabrication steps. Note that in Figure 2 an additional dielectric film 13 is deposited over the exposed surface of the

epitaxial layer 44. This serves, in part, to provide insulation for metallization layer 46.

Integrated circuit devices can optionally be fabricated in the circuit device grade epitaxial layer prior to the formation of the insertion structures. This circuit device grade epitaxial layer formed in the manner described above allows ICs to be fabricated with insertion structures integral to the substrate of the IC (die) and that extend from the bottom of the thinned semiconductor substrate (epitaxial layer). Such devices are described below in connection with Figures 5b and 7. Integral insertion structures simplify the mechanical handling in testing, burn-in and packaging of the IC to a two step process consisting of physical alignment and the application of a loading force. ICs with an integral insertion structure also allows three-dimensional IC structures to be assembled as shown in Figure 7.

Figure 3 further illustrates an insertion structure 10' that is shaped generally like an obelisk which may be formed by a combination of dry and wet etching. The nearly vertical walls 50 of insertion structure 10' are formed by first dry etching the substrate 44. Walls 50 are then passivated prior to wet etching tip portion 18 as described above.

Figure 4a illustrates an insertion structure device 60 used as a circuit probe for integrated circuit 62 during functional circuit testing or electrical burn-in. Integrated circuit 62, which may still be in wafer form, is supported on a holding fixture 64. Device 60 is formed on a thin flexible

membrane 66, supported at its perimeter by retaining ring 67. Circuit 62 is brought into alignment with device 60 in the horizontal plane such that the insertion structures of device 60 are disposed above the corresponding contact pads of the circuit. A suitable force application means 68 is applied to the back side of flexible membrane 66 so that the insertion structures of device 60 make electrical contact with the corresponding circuit pads. A mechanical means for applying force is represented in Figure 4a; however, any other means, such as pressurized fluid, could also be used. Typically, a loading force of less than 5 gms per insertion structure is sufficient to establish a reliable contact.

Burn-in of circuit devices typically requires many hours of testing under stressing temperature and electrical conditions. A die that passes this testing is subsequently packaged in some manner, so it is important that the electrical contact made to the contact pad of the die during burn-in be temporary with minimal or no visible damage to the pad of the die. The benefits of a burn-in fixture made in accordance with the present invention are the ability to process the die while in wafer form, to do so without damage to the pads of the die, to test the die at or near the full speed operating speed of the circuit (owing to the IC fabrication method of the membrane), all at a low cost in capital equipment fixturing.

Figure 4b illustrates an insertion structure device 160 that is particularly adapted for functional testing and/or electrical burn-in of a full wafer fabricated semiconductor 162. Wafer 162 is supported by a fixture

or wafer chuck 164. Device 160 is formed on a membrane 166 and includes a set of insertion structures for each integrated circuit die on wafer 162 that is to undergo testing and/or burn-in. Insertion structures corresponding to the contact pads of each die are appropriately coupled to signal, power and ground traces formed in layers of metallization deposited on and through membrane 166. These traces terminate at connectors at the periphery of membrane 166 where it is supported by ring 167. The peripheral connectors are electrically coupled by conventional means to test electronics such that each die of wafer 162 can be individually powered, accessed and tested. Device 160 is held in tooling 168 which is mechanically aligned with wafer chuck 164. The insertion structures of device 160 are brought into contact with mating pad on wafer 162 by suitable force application means (not shown).

Figure 5a illustrates an insertion structure device 70 with a rigid backing substrate 71 used as a circuit testing or burn-in fixture for integrated circuit 72. Contact pads of circuit 72 are aligned with mating insertion structures of device 70 and a sufficient force is applied (by means not shown) to establish electrical contact without forming permanent bonds. Device 70 preferably includes integral circuitry 74 to control its operation and to provide electrical communication between the insertion structures and bonding pads 76 disposed at the periphery of device 70.

Figure 5b illustrates a circuit testing or burn-in fixture 80 similar to that shown in Figure 5a; however, in this case, circuit 82 is fabricated with

integral insertion structures and mating contact pads are fabricated on the surface of fixture device 80. As in the previous example, integral circuitry 84 is preferably fabricated directly on device 80.

Figure 6 illustrates an insertion structure device 90 used as a permanent mounting structure for integrated circuit 92. In this case, permanent metallic bonds are formed, for example in the manner illustrated in Figure 1c, between the insertion structures of device 90 and the corresponding pads of circuit 92. The insertion structures are electrically connected to the pins 94 of package 96 by means of (active or passive) integral circuitry 98 formed directly on device 90. It will be recognized that a similar packaging solution may be achieved using a circuit having integral insertion structures and a substrate having mating contact pads in a manner analogous to that shown in Figure 5b.

Figure 7 illustrates a three-dimensional integrated circuit fabricated with the techniques of this invention. Each of circuit devices 100a-100d is fabricated with an array of integral insertion structures on one surface and with an array of contact pads on the opposite surface. The array of contact pads on each device corresponds to the array of insertion structures on the device stacked above, and the devices are permanently bonded to one another. The stack of devices is supported on a substrate 102 which may be packaged in the manner illustrated in Figure 6. It will be recognized that this technique is capable of achieving an extremely high circuit density within a single package.

Figure 8 illustrates an insertion structure 120 formed in the same manner as structure 10 of Figure 1a but using a rectangular etching window to produce an elongated insertion structure with a blade-like edge 122. The length of edge 122 is not restricted, but would typically be less than approximately 2 mils (50μm).

Figure 9 illustrates yet another form of insertion structure 130. In this case, a circular etching window is used to provide a circular cross-section. Alternatively, an oval window could be used to provide a corresponding oval cross-section. A controlled dry etch process is used to form inclined (conical) side walls 132 and a concave tip portion 134. Insertion structure 130 thus has a piercing or cutting edge 136 around the entire periphery of tip portion 134. The concave shape of the tip is a result of the dry etch process control. This form of insertion structure increases the metal-to-metal contact area that the insertion structure has with the circuit pad to be controlled.

It will be recognized that the above described invention may be embodied in other specific forms without departing from the spirit or essential characteristics of the disclosure. Thus, it is understood that the invention is not to be limited by the foregoing illustrative details, but rather is to be defined by the appended claims.

CLAIMS

I claim:

1. A device for making electrical contact with an integrated circuit having at least one metallized circuit pad, said device comprising:

(a) a supporting substrate;

(b) at least one insertion structure supported by the substrate and projecting therefrom, said insertion structure having a base portion proximal to the substrate and a tip portion at a distal end of the insertion structure;

(c) a layer of conductive material disposed on the tip portion of the insertion structure;

(d) conduction means coupled to the layer of conductive material for providing an electrically conductive path to the tip portion of the insertion structure.

2. The device of claim 1 wherein the side walls of the insertion structure comprise a layer of dielectric material.

3. The device of claim 2 wherein the dielectric material is selected from the group consisting of silicon nitride and silicon dioxide.

4. The device of claim 1 wherein a plurality of insertion structures are disposed on the supporting substrate in mating alignment with a corresponding plurality of circuit pads on the integrated circuit.

5. A method of fabricating a device for making electrical contact with an integrated circuit comprising the steps of:

(a) depositing a mask layer on a surface of a sacrificial substrate;

(b) etching a pattern of apertures through the mask layer;

(c) etching the sacrificial substrate exposed by the pattern of apertures to form a pattern of wells with tapering side walls;

(d) depositing a layer of conductive material within each of the wells;

(e) depositing a layer of dielectric material over the structure formed in step (d);

(f) etch removing the sacrificial substrate to expose at least a tip portion of the conductive material deposited within each of the wells, thereby forming a pattern of projecting insertion structures.

6. The method of claim 5 wherein the sacrificial substrate is silicon.

7. The method of claim 6 wherein the silicon has a <100> crystal orientation.

8. The method of claim 5 wherein the dielectric material is selected from the group consisting of silicon dioxide and silicon nitride.

9. The method of claim 8 wherein the dielectric material has a tensile stress of approximately 1×10^8 dynes/cm^2.

10. The method of claim 9 wherein the dielectric material is deposited to form the mask layer.

11. The method of claim 5 wherein the sacrificial substrate is entirely removed in step (f).

12. The method of claim 5 further comprising the step of forming an etch stop layer on the sacrificial substrate followed by the step of forming a semiconductor layer over the etch stop layer and then removing the sacrificial substrate in step (f) to the etch stop layer.

13. The method of claim 12 further comprising the step of removing the etch stop layer.

14. The method of claim 13 further comprising the step of fabricating an integrated circuit on said semiconductor layer.

15. The method of claim 12 wherein the etch stop layer is an epitaxial layer.

16. The method of claim 15 wherein the etch stop layer is germanium-boron doped silicon.

17. The method of claim 16 wherein the etch stop layer has a dopant concentration of approximately 2 x 10^{20}boron atoms/cm^3.

18. The method of claim 15 wherein the semiconductor layer is an epitaxial layer.

19. A method of fabricating an integrated circuit with integral insertion structures comprising the steps of:

(a) forming an etch stop layer on a semiconductor substrate;

(b) forming a circuit grade semiconductor layer over the etch stop layer;

(c) depositing a mask layer on an exposed surface of the circuit grade semiconductor layer;

(d) etching a pattern of apertures through the mask layer;

(e) etching a pattern of wells with tapering side walls into the semiconductor substrate underlying the pattern of apertures;

(f) depositing a layer of conductive material within each of the wells;

(g) depositing a layer of dielectric material over the structure formed in step (f);

(h) etch removing the semiconductor substrate to the etch stop layer to expose at least a tip portion of the conductive material deposited within each of the wells, thereby forming a pattern of projecting insertion structures;

(i) removing the etch stop layer to expose the circuit grade semiconductor layer.

20. The method of claim 19 wherein the semiconductor substrate is silicon.

21. The method of claim 20 wherein the silicon has a <100> crystal orientation.

22. The method of claim 18 wherein the dielectric material is selected from the group consisting of silicon nitride and silicon dioxide.

23. The method of claim 22 wherein the dielectric material has a tensile stress of approximately 1×10^8 dynes/cm^2.

24. The method of clam 23 wherein the dielectric material is deposited to form the mask layer.

25. The method of claim 19 wherein the etch stop layer is an epitaxial layer.

26. The method of claim 25 wherein the etch stop layer is germanium-boron doped silicon.

27. The method of claim 26 wherein the etch stop layer has a dopant concentration of approximately 2 x 10^{20}boron atoms/cm3·

28. The method of claim 19 wherein the circuit grade semiconductor layer is an epitaxial layer.

29. The method of claim 28 further comprising the step of fabricating an integrated circuit on said circuit grade semiconductor layer.

30. A device for electrically activating an integrated circuit having a plurality of metallized contact pads, said device comprising:

(a) a supporting substrate;

(b) a plurality of insertion structures supported by the substrate and projecting therefrom in mating alignment with corresponding ones of the plurality of contact pads on the integrated circuit, each of said insertion structures having a base portion proximal to the substrate, a tip portion at a distal end of the insertion structure, and side walls tapering from the base portion toward the tip portion;

(c) a layer of conductive material disposed on the tip portion of each of the insertion structures;

(d) conduction means coupled to the layer of conductive material of each insertion structure for providing an electrically conductive path to the tip portion of the insertion structure;

(e) force application means coupled to the supporting substrate for urging the plurality of insertion structures into intimate contact with the corresponding plurality of contact pads, thereby establishing electrical communication therewith.

31. The device of claim 30 wherein the integrated circuit comprises a full wafer having a plurality of integrated circuit dice and the device includes insertion structures for contacting each die of the full wafer.

32. A device for mounting an integrated circuit having a plurality of metallized contact pads, said device comprising:

(a) a supporting substrate;

(b) a plurality of insertion structures supported by the substrate and projecting therefrom in mating alignment with and bonded to corresponding ones of the plurality of contact pads on the integrated circuit, each of said insertion structures having a base portion proximal to the substrate, a tip portion at a distal end of the insertion structure penetrating into the corresponding contact pad, and side walls tapering from the base portion toward the tip portion;

(c) a layer of conductive material disposed on the tip portion of each of the insertion structures;

(d) conduction means coupled to the layer of conductive material of each insertion structure for providing an electrically conductive path to the tip portion of the insertion structure, thereby establishing electrical communication with the corresponding contact pad.

33. An integrated circuit device comprising:

(a) an integrated circuit formed on a semiconductor substrate having a plurality of apertures therethrough;

(b) a plurality of insertion structures disposed within respective ones of the plurality of apertures and projecting therefrom, each of said insertion structures having a base portion proximal to the substrate and a pointed tip portion at a distal end of the insertion structure;

(c) a layer of conductive material disposed on the tip portion of each of the insertion structures;

(d) conduction means coupled to the layer of conductive material of each insertion structure for providing an electrically conductive path between the tip portion of the insertion structure and a corresponding node of the integrated circuit.

34. An electronic device comprising a plurality of integrated circuit devices each of which has a first and second surface and comprises:

(a) an integrated circuit formed on a semiconductor substrate having a plurality of apertures therethrough;

(b) a plurality of insertion structures disposed within respective ones of the plurality of apertures and projecting from the first surface of

the integrated circuit device, each of said insertion structures having a base portion proximal to the substrate and a pointed tip portion at a distal end of the insertion structure;

(c) a layer of conductive material disposed on the tip portion of each of the insertion structures;

(d) first conduction means coupled to the layer of conductive material of each insertion structure for providing an electrically conductive path between the tip portion of the insertion structure and a corresponding node of the integrated circuit;

(e) a plurality of contact pads disposed on the second surface of the integrated circuit device;

(f) second conduction means coupled to each of the contact pads for providing an electrically conductive path between the contact pad and a corresponding node of the integrated circuit;

wherein the plurality of integrated circuit devices are stacked with the tip portions of the insertion devices of one such integrated circuit device in mating contact with crresponding contact pads of an adjacent integrated circuit device.

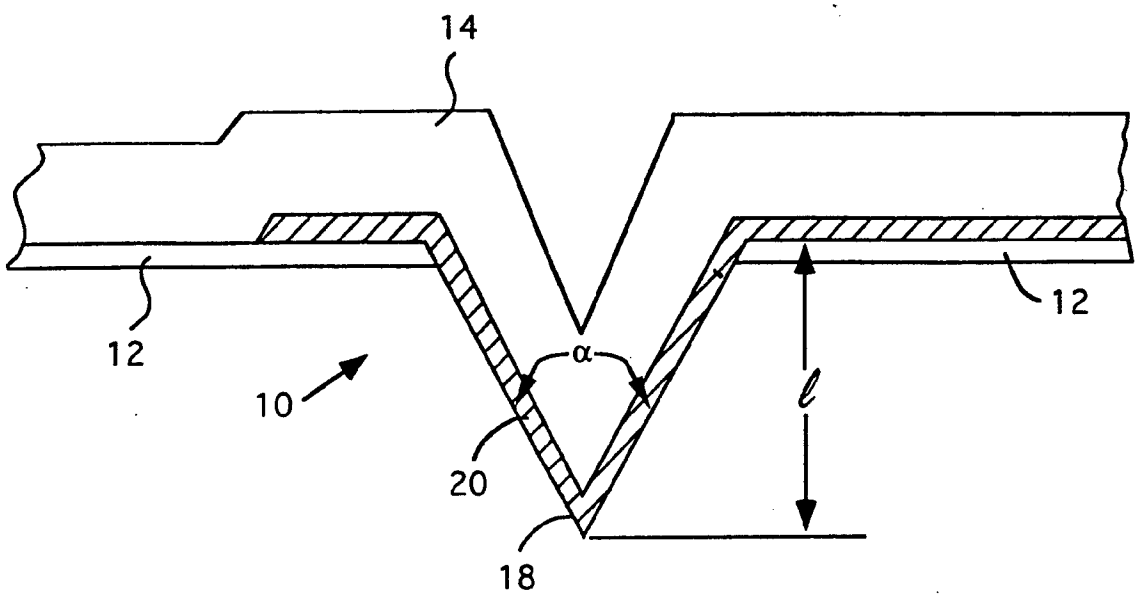

Fig_1a

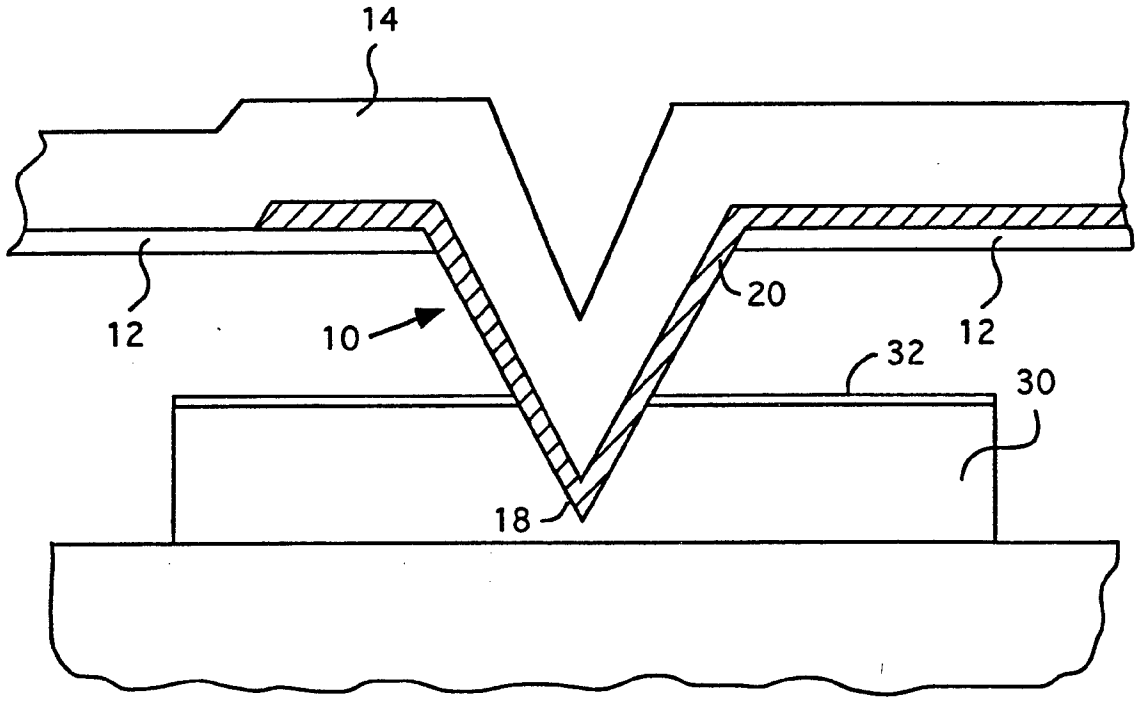

Fig_1b

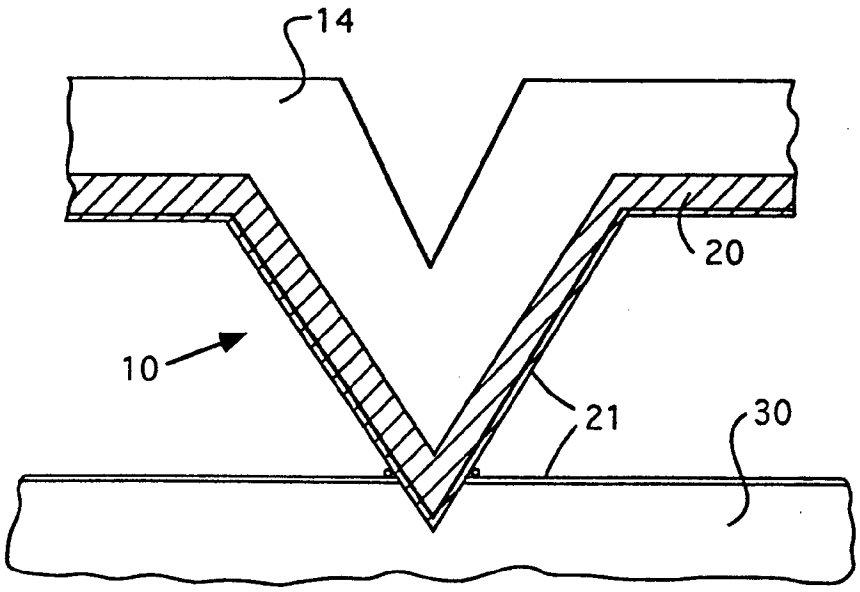

Fig_1c

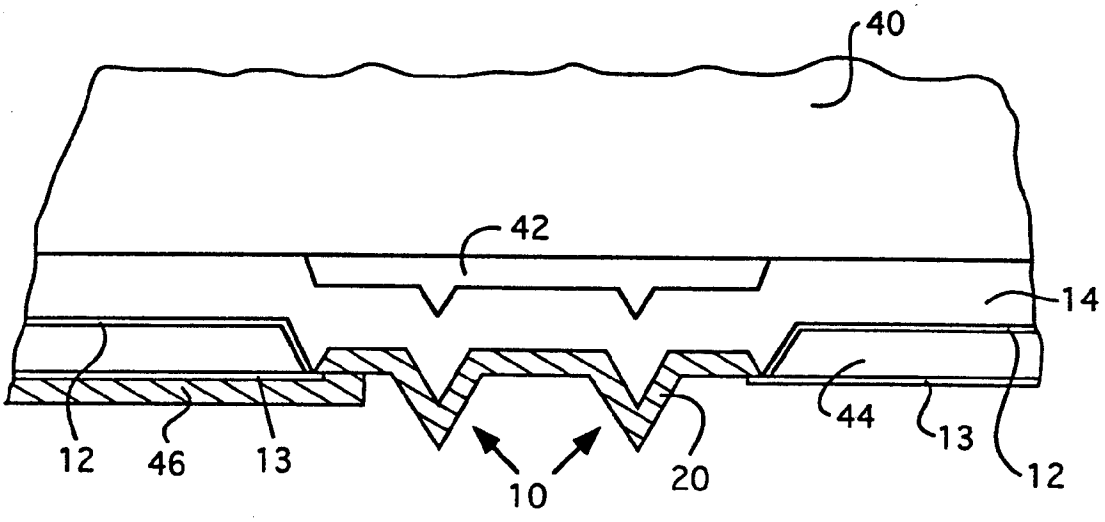

Fig_2

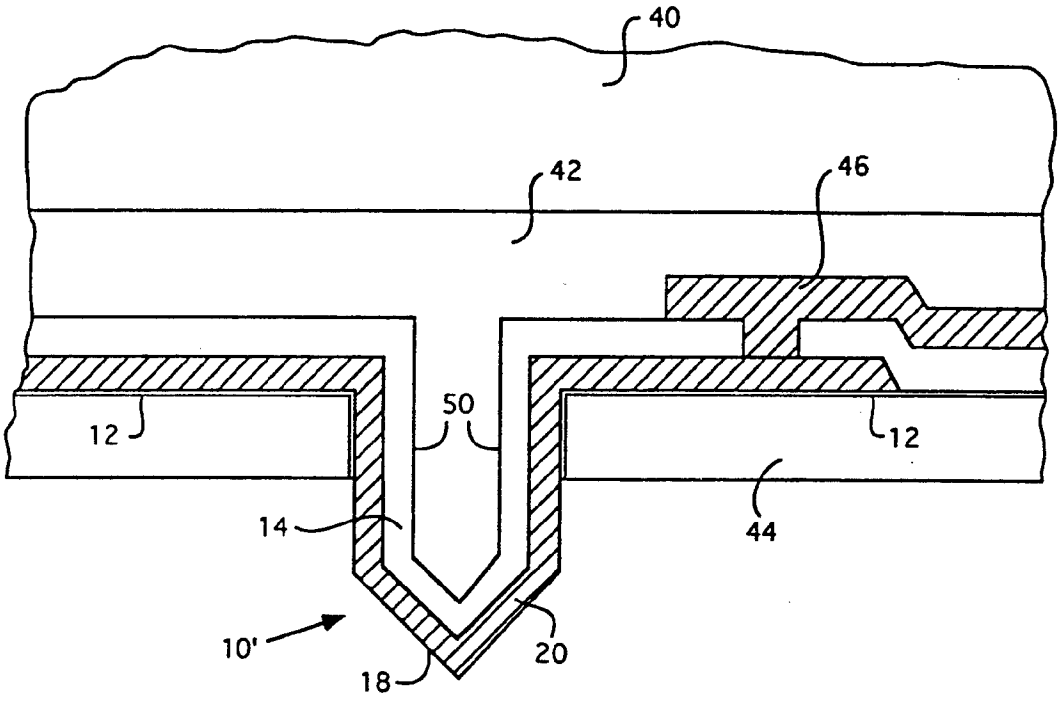

Fig_3

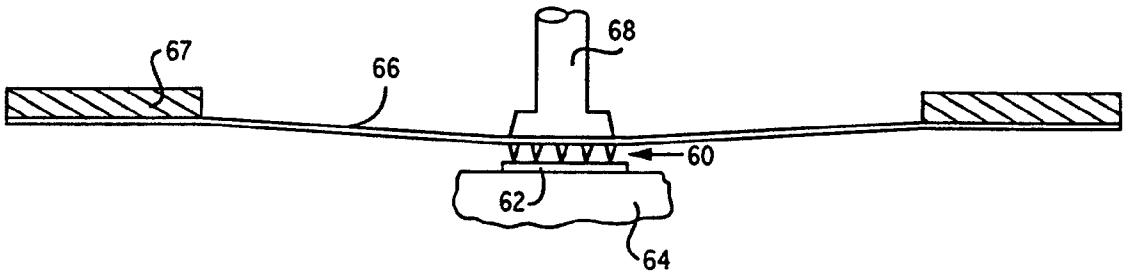

Fig_4a

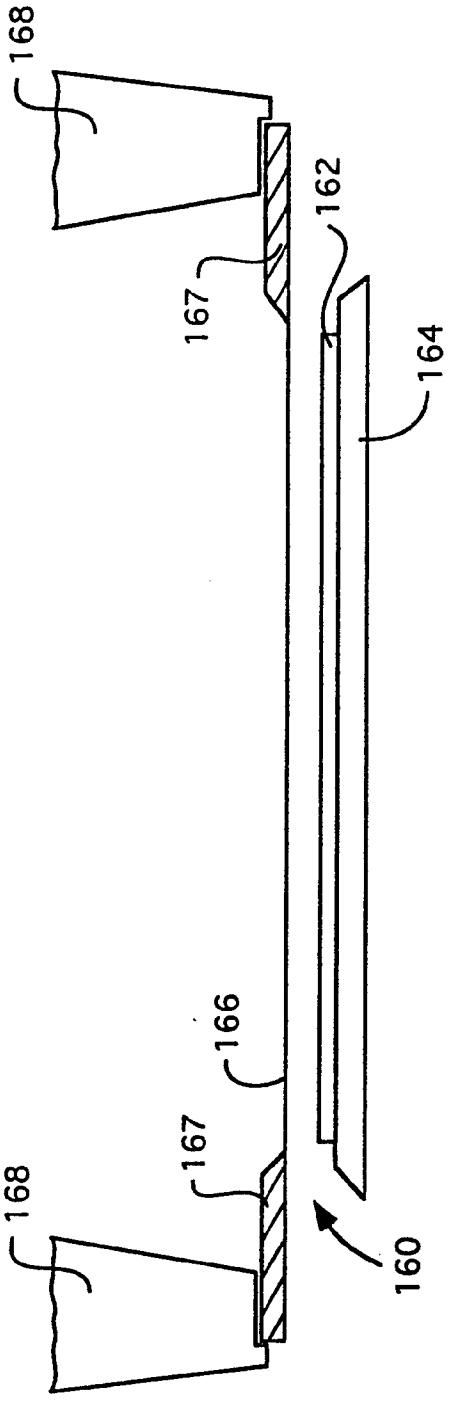

Fig_4b

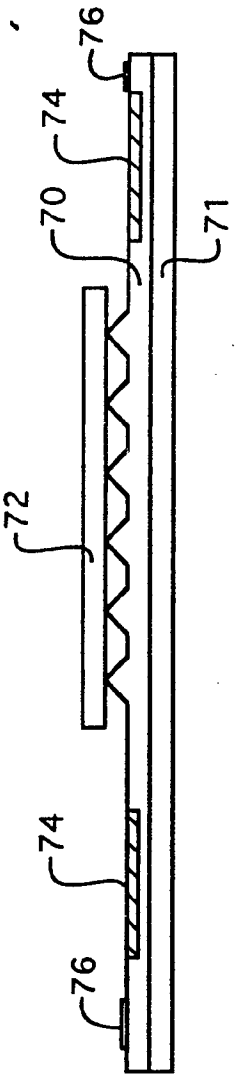

Fig_5a

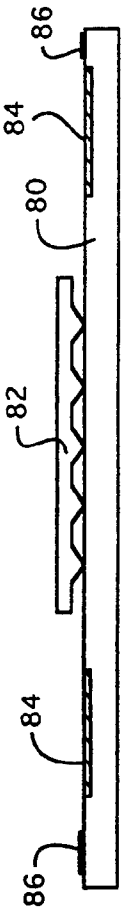

Fig_5b

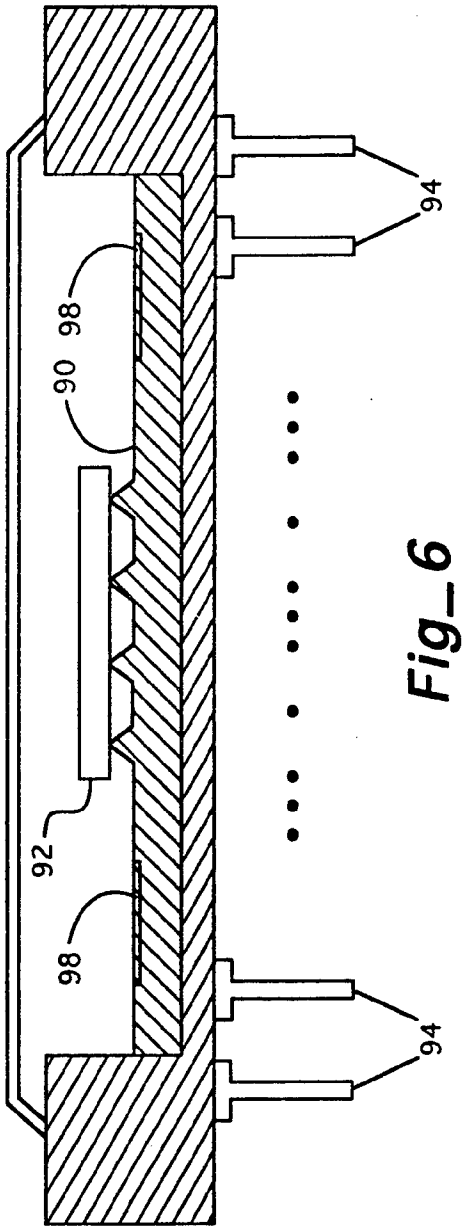

Fig_6

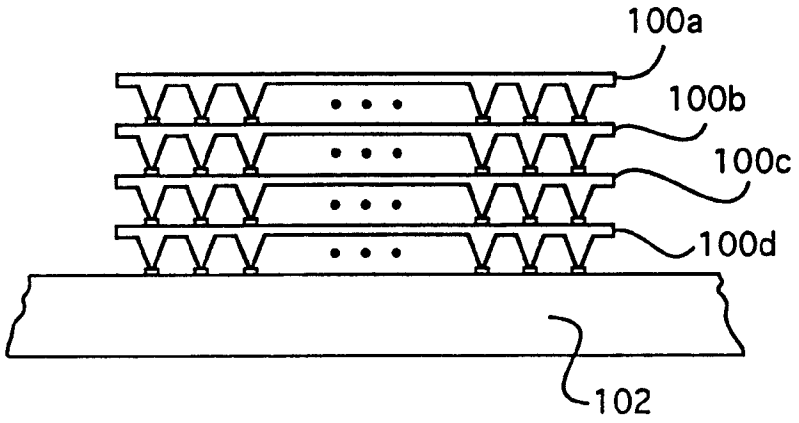

Fig_7

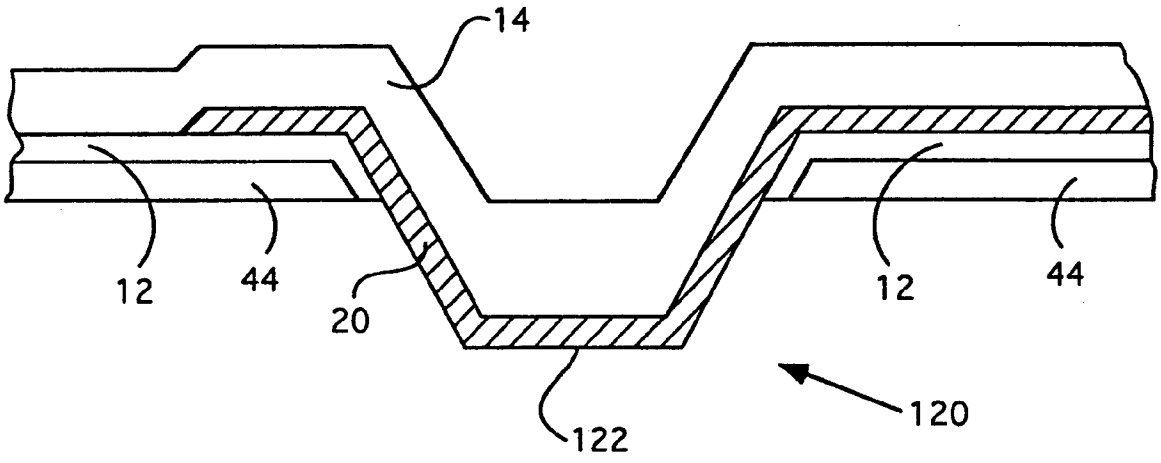

Fig_8

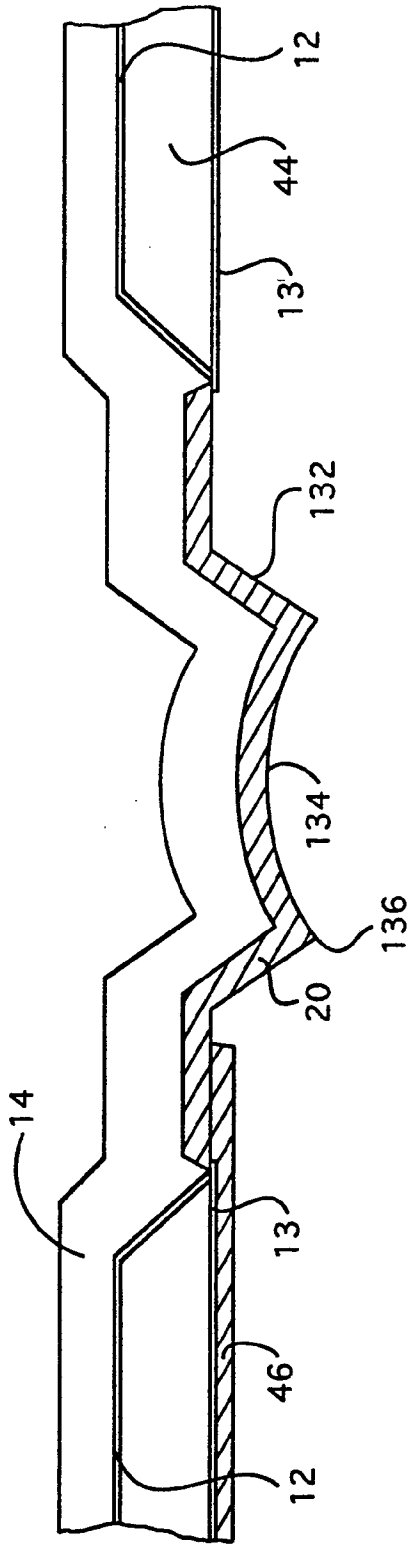

Fig_9

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/09709

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :H01L 23/48, 29/44, 29/52, 29/60, 29/46, 29/62
US CL :257/750, 751, 753, 748, 437/187, 189, 203, 204, 190
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 257/750, 751, 753, 748, 437/187, 189, 203, 204, 190

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A 4,862,243 (WELCH et al), 29 August 1989, See entire document.	1-4, 30-34
A	US, A 5,048,744 (CHANG et al), 17 September 1991, see entire document.	1-4, 30-34
Y	US, A 2,909,715 (ADCOCK), 20 October 1959, see entire document.	1-34
Y	US, A 3,458,778 (GENZABELLA et al), 29 July 1969, see entire document.	1-34

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be part of particular relevance

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"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search
20 December 1993

Date of mailing of the international search report
27 DEC 1993

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